**18CS203J- Computer Organisation and Architecture**

**Easy Questions**

1. Methodology by which performance improved by executing two or more tasks simultaneously is :
   1. Collaborative processing
   2. **Parallel Processing**
   3. Concurrent Processing
   4. Simultaneous processing
2. Technique towards reducing the amount of time needed to wait for a particular task to be solved in parallelism is:
   1. **Increasing computational Speed**
   2. Increasing performance
   3. Increasing throughput
   4. Latency reduction
3. Technique towards completing number of process or tasks in a given unit of time is
   1. **Enhancing the throughout**
   2. Enhancing the process
   3. Enhancing Tasks
   4. Reduction of processing time
4. Type of parallelism where data is distributed across different nodes in parallel are called
   1. Instruction level
   2. **Data Level**
   3. Task level
   4. Transaction level
5. Which type of parallelism does not depend on each other for execution ?
   1. **Instruction level**
   2. Task Level
   3. Transaction Level
   4. Data Level
6. Data-level parallelism / task-level parallelism in a tightly coupled equipment which permits communication among parallel threads, are handled by
7. Instruction-Level Parallelism
8. Request-Level Parallelism
9. **Thread-Level Parallelism**
10. Vector Architectures and Graphic Processor Units
11. The do not have parallel processing capabilities
12. **Single Instruction stream, Single Data stream**
13. Single Instruction stream, Multiple Data stream
14. Multiple Instruction stream, Multiple Data stream
15. all of the above
16. Type of computer where a single instruction would operate or execute on multiple data values by sharing common memory is called
17. **Single Instruction stream, Multiple Data stream**
18. Single Instruction, Single Data Stream
19. Multiple Instruction, Single Data Stream
20. Multiple Instruction, Multiple Data Stream
21. Type of threading which switches between threads on each instruction is called
    1. **Fine Grained** (b)Coarse Grained

(c)Simultaneous (d)All of above

1. Type of machines which got equal access and access times to memory are:
   1. **Uniform Memory Access (UMA)**
   2. Cache Coherent UMA
   3. Non-Uniform Memory access (NUMA)
   4. COMA
2. In memory chip, each memory cell can hold how many much of information

**(a)1 bit**

1. 1 byte
2. 2 Kilo byte
3. 1 megaByte
4. In memory chip, all cells in row are connected to a common line called
   1. **Word line** (b)Control line

(c)Read line (d)MUX

1. MESI Protocol is a sort of inquisitive **(a.) Cache protocol**

(b.) Processor protocol (c.) Memory protocol (d.) Instruction protocol

1. In MESI Protocol, state specifies that the cache line is existing in current cache only and its significance is diverse from the main memory.

**(a)Modified**

1. Exclusive
2. shared
3. Invalid
4. In SRAM cell for reading state, Switches T1 and T2 are in (a)**Closed state**
5. Open
6. Grounded
7. none
8. In which mapping, the data can be mapped anywhere in the cache memory?
   1. **Associative**
   2. Direct
   3. Set Associative
   4. indirect
9. Which of the memory chips are volatile ? (a)SRAM
10. DRAM
11. **SRAM and DRAM**
12. EPROM
13. Which of memory allows the data to be erased and loaded by reprogramming ROM? (a)**EPROM**
14. PROM
15. EEPROM
16. FLASH
17. Cache memory
18. has greater capacity than RAM
19. is faster to access than CPU Registers
20. is permanent storage
21. **is faster to access than RAM**
22. Type of memory for increasing the size of the memory system is called (a)**Virtual Memory**
    1. Cache Memory
    2. L1 Cache
    3. L2 Cache



**Moderate Questions**

1. The instruction is said to be in while it is between its start and end of its running phase.

(a). **Execution**

1. Wait
2. Stall
3. Branching
4. Which class of systems belongs to von Neumann computer? (a). SIMD (Single Instruction Multiple Data)

(b). MIMD (Multiple Instruction Multiple Data) (c). MISD (Multiple Instruction Single Data) (d.) SISD (Single Instruction Single Data)

Answer: (d)

1. SIMD symbolizes an organization that.
   1. refers to a computer system capable of processing several programs at the sametime.
   2. represents organization of single computer containing a control unit, processorunit and a memory unit.
2. Includes many processing units under the supervision of a common controlunit.
3. None of the above Answer: (c)
4. Multiple tasks executing independently is called as (a). Multithreading

(b). Multiprogramming

(c) . Multitasking (d.) Synchronization

Answer: (b)

1. Which is the suitable one for increasing processor word size in a parallelism. (a). Increasing

(b). Count based (c). Bit based (d). Bit level

Answer: (d)

1. The cost of a parallel processing can be resolute by (a). Time Complexity

(b). Switching Complexity

(c) Circuit Complexity (d). None of the above

Answer: (c)

1. Flynn’s Classification discriminates multi-processor computer structural design rendering to

(a). Independent dimensions of Instruction stream and Data stream (b). Dependent dimensions of Instruction stream and data stream. (c). Independent dimensions of memory and processor.

(d). Dependent dimensions of memory and I/O stream.

Answer: (a)

1. A write is only performed liberally in MESI protocol, if the cache line is in (a). Either Modified or Exclusive state
2. Modified state only
3. Shared state or Invalid state (d). Shard state only

Answer: (a)

9.\_\_\_\_\_\_\_\_ ensures write back caches.

(a). MOSI protocol

(b) MOESI protocol (c). MESI protocol

(d) MSI protocol Answer: (c)

1. \_\_\_\_\_\_\_\_\_\_\_\_is a full cache coherence protocol that encompasses all of the possible states commonly used in other protocols.
2. MOESI protocol
3. MESI protocol
4. MSI protocol
5. MOSI protocol Answer: (b)
6. When a processor needs to read a block which none of the other processors have and then write to it, the MESI protocol uses .
7. Shared
8. Exclusive
9. Invalid
10. Owned Answer: (b)
11. A cache line in \_\_\_\_\_\_\_\_\_\_state does not hold a valid copy of data with respect to MESI protocol.

(a). Shared (b). Exclusive (c). Invalid (d). Owned

Answer: (c)

1. Which cache write mechanism allows an updated memory location in the cache to remain out of date in memory until the block containing the updated memory location is replaced in the cache?
2. Write through
3. Write back
4. Both write through and write back
5. Cycle Stealing Answer: (b)
6. Assume the data bus width of DDR memory system is 32 bits. How many cycles does it take to transfer 64B cache block?
7. 64
8. 16
9. 8
10. 1 Answer: (c)
11. The Translation Look Aside Buffer (TLB) stores (a)Branching data
    1. Map of Cache data and RAM data
    2. Map of Physical Address and Logical Address (d)Memory Translation times

Answer: (b)

1. Page fault occurs when
2. requested page is in memory
3. a requested page is not in memory
4. a page is corrupted
5. None of the above Answer: (b)
6. Of the following, which best characterizes computers that use memory-mapped I/O?
7. The computer provides special instructions for manipulating I/O ports.
8. I/O ports are placed at addresses on the bus and are accessed just like other memorylocations.
9. To perform an I/O operation, it is sufficient to place the data in an address register and call thechannel to perform the operation.
10. Ports are referenced only by memory-mapped instructions of the computer and are located athardwired memory locations.

Answer: (b)

1. In dynamic memory chip, technique for reducing the number of pins are: (a)Multiplexing addresses
   1. Reducing address lines
   2. Address Decoder (d)Encoder

Answer: (a)

1. From Among the following, which has the biggest largest memory size?

(a)Registers

1. Magnetic Disk
2. Memory (d)Cache

Answer: (b)

1. Techniques for improving hit rate are :
2. Increasing block size
3. Increasing block size with constant cache size
4. Increasing cache memory (d)Increasing main memory

Answer: (b)

1. Process of bringing the data before Read miss occurs is (a)Prefetching
2. Fetching
3. Executing
4. Read hit Answer: (a)
5. Which among the following is true?
6. The memory allocated to each page is contiguous.
7. The offset is different in a virtual address and a physical address
8. Logical address space can be smaller than physical address space\
9. Segmentation avoids external memory fragmentation Answer: (a)
10. The starting address of a page table in kept in
11. Main Memory
12. Cache Memory
13. Register
14. Page Table Base Register Answer: (d)
15. Memory management technique in which system stores and retrieves data from secondary storage foruse in main memory is called

(a)Fragmentation (b)Paging

(c)Mapping (d)Indexing

Answer: (b)

1. Which of following refers to programme Controlled I/O
2. JMP
3. BR
4. CMP
5. All of Above Answer: (d)

Difficult

1. Consider an instruction as follows: A= (L1\*L2) + (L3\*L4)

B= (L1\*L2) - (L3\*L4)

So for this compute the software and hardware parallelism and show diagrammatically cycles.//Question is unclear. How to show diagrammatically?

(a) 2.67 and 1.14

(b) 2.67 and 1.0

(c) 2.5 and 1.14

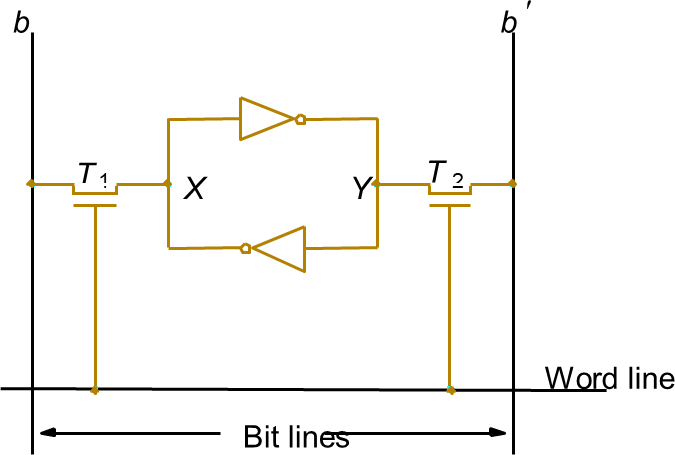
(d) 2.55 and 1.14

Answer: (a)

1. Let us assume we want to sum all the elements of the given array of size 10 and the time for a single addition operation is 2 time units. If we execute this job as a data parallel job on 4 processors the time taken would reduce be what ? Assuming merging overhead time unit is 5 time units
   1. 10 time units
   2. 5 time units
   3. 15 time units
   4. 7 time units Answer: (a)
2. Consider a 4 core processor named as Core 1, Core 2, Core 3, and Core 4. Main memory is holding data say X= 1500H. Core 1 reads value of X which is 1500H. Core 2 also read same value of X which is 1500H. Core 1 writes to X which is 3000

H. Core 2 attempts to read X which is old copy i.e 1500H. What kind of problem it is and solution to it is

1. Cache Coherence and invalidation is done where copies of X in other caches are invalidated.
2. Cache miss
3. Cache coherence and snooping done to monitor the bus connecting cores
4. (a) or (c) Answer: (d)
5. Consider the circuit given below. For read operation, what should be done



* 1. Switches T1 and T2 are grounded
  2. Switch T1 and T2 are closed by activating the word line
  3. Sense/Write circuits monitor the status of b and b’
  4. (b) and (c) Answer: (d)

1. Consider a situation where a device requests for service by sending a special code to the processor. Based on code, the device identified by the processor and interrupt here produces a call to predetermined memory location , which is the starting address of ISR. Such interrupts refer to what.
   1. Polling
   2. Priority interrupt
   3. Vectored Interrupt
   4. All of Above Answer: (c)

**CT3 -QUESTIONS**

**PART A**

1. Executing two or more operations at the same time is known as --------

1. Distributed processing
2. Pipe processing
3. Parallel processing
4. multi processing

2 displays the patterns of simultaneously executable operations.

1. flow graph
2. program flow graph
3. program flow chart
4. flow chart
5. consider the instructions

A=X1\*X2+X3\*X4

B=X1\*X2-X3\*X4 How many load instructions required for this?

1. 8
2. 4
3. 2

d)1

1. Hardware Parallelism can be achieved through
2. Parallel processor
3. multi processor
4. k-issue processor
5. pipeline processor
6. TWO-issue processors are capable of doing-------------
7. one memory access(Load/Store) and two arithmetic operation
8. two memory access(Load/Store) and one arithmetic operation
9. two memory access(Load/Store) and two arithmetic operation
10. one memory access and one arithmetic operation
11. Executing several instructions per clock cycle is \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_while overlapping of multiple instructions is

.

1. Parallel processor, pipeline processor
2. multi processor, pipeline processor
3. pipeline processor, k-issue processor
4. pipeline processor, Parallel processor
5. Which of the following is true?
6. pipeline processors have lower performance than Parallel processor
7. Parallel processors have lower performance than pipeline processor
8. Parallel processors and pipeline processor have lower performance
9. Parallel processors and pipeline processor have more performance pipeline processor

8 Pushes only one instruction to next stage / clock cycle.

1. Parallel processors
2. pipeline processors
3. multi processors
4. k-issue processors
5. What type of hazards are identified in the following instructions ? x= a+b ; y=c-d; z=x \* y
6. Data hazards
7. Control Hazards. c)Instruction Hazards.

d) pipeline Hazards.

1. plays an important part in evaluating the performance of a data parallel programming model.
   1. Locality of Reference
   2. memory Reference
   3. data reference
   4. instruction reference
2. Flynn's taxonomy are based on----------------------
3. main memory size
4. the number of concurrent instruction and data
5. cache memory size
6. both on (a) and (c)
7. does not have parallel processing capabilities a)SIMD

b)SISD c)MISD d)MIMD

1. Which of the following holds true with respect to Cache memory
2. It has greater capacity than RAM
3. It is faster to access than CPU Registers
4. It is permanent storage
5. It is faster to access than RAM
6. Most commonly used cache coherence protocol is a)MOESI protocol
7. MESI protocol
8. MSI protocol
9. MOSI protocol
10. A thread comprises of
11. Thread id
12. program counter
13. stack, and a set of registers
14. All of the above
15. In Hardware Multithreading execution of multiple thread is supported by
16. CPU
17. OS
18. Cache
19. None of the above
20. Cache Coherence Problem arises with respect to a)Sharing of writable data.

b) updating data in cache. c)Inconsistency due to I/O d)All of these

1. Switches between threads on each instruction is happened in
2. multi threading
3. coarse grained multi threading
4. Fine grained multi threading
5. Fine and coarse grained multi threading
6. Which of the following holds true in the context of multicore processors?
7. They are MIMD
8. all cores share the same memory
9. They are shared memory multiprocessor
10. all the above
11. In NUMA, the Shared memory that is physically distributed among all the processors are called ------
12. local memories.
13. remote memories.
14. cache memories.
15. None of the above

**PART B**

1. Consider the instructions

A=X1\*X2+X3\*X4

B=X1\*X2-X3\*X4 How many machine cycles required for the parallel execution? (consider the Software Parallelism)

1. 12
2. 4
3. 6
4. 3
5. Consider the instructions

A=X1\*X2+X3\*X4

B=X1\*X2-X3\*X4 How many machine cycles required for the parallel execution? (consider the H/W Parallelism with 2-issue processor)

1. 12
2. 4
3. 7
4. 3
5. How much units of time required to complete the following operationswhen they are executed in Instruction level parallelism manner?

x= a+b ; y=c-d; z=x \* y a)2

1. 4
2. 1
3. 3
4. Which of the following holds true with respect to UMA and NUMA?
   1. No memory controller in UMA and NUMA
   2. single memory controller in NUMA and multiple memory controller in UMA
   3. Multiple memory controller in UMA and multiple memory controller in NUMA
   4. single memory controller in UMA and multiple memory controller in NUMA
5. Processors have their own local memory and operates independently are called a)Distributed memory computers
6. ccNUMA systems
7. nccNUMA systems d)Symmetric multiprocessors
8. which of the following is correct w.r.to these instructions

(i) x= a+b ; (ii) y=c-d; (iii) z=x \* y

1. (i) and (ii) can be computed simultaneously.
2. (i) and (ii) cannot be computed simultaneously.
3. (iii) cannot be calculated until (i) and (ii) are calculated
4. both (a) and (c) are correct
5. which of the following ensures data consistency between the cache memory and the shared memory a)bus protocol
6. SI protocol
7. **Snoopy bus protocols**
8. **seven layer** protocol
9. The policies used for maintaining cache consistency by **Snoopy bus protocols are** .
   1. Write-invalidate policy
   2. Write-read policy
   3. Write-update policy
   4. both (a) and (c)
10. Invalidate/ **dirty** bit in Write-invalidate policy represent
    1. they can be used in near future
    2. they should not be used at all
    3. they can be modified
    4. they cannot be modified
11. Under which policy, the processor that is writing the data can broadcasts the new data over the bus without issuing the invalidation signal
12. Write-invalidate policy
13. Write-read policy
14. Write-update policy
15. both (a) and (c)
16. includes many processing units under the supervision of a common control unit.

a)SIMD b)SISD c)MISD

d)MIMD

1. is always performed in local cache memory without causing a transition of state
2. Read Miss
3. Write Hit
4. Read Hit
5. Write Miss

13 ) locality of reference in the memory systems are

a) Temporal b)spatial c)sequential

d) All of the above

1. MROM (mask ROM) and **PROM (programmable ROM) stands**
   1. Mask ROM and Parallel ROM
   2. Memory ROM and Programmable ROM
   3. Mask ROM and Programmable ROM
   4. None of the above
2. Cache between main memory and processor and caches on the processor chip and are
3. L2 and L1
4. L1 and L2
5. L1 and L3
6. L2 and L3
7. Page fault occurs when
8. a requested page is in memory
9. a requested page is not in memory
10. a page is corrupted
11. None of the above
12. In which mapping, the data can be mapped anywhere in the cache memory? a)Associative
13. Direct
14. Set Associative d)Indirect
15. Which cache write mechanism allows an updated memory location in the cache to remain out of date in memory until the block containing the updated memory location is replaced in the cache?
16. Write through
17. Write back
18. Both write through and write back
19. Cycle Stealing
20. is the memory access where all the processors share the physical memory in a centralized manner with

equal access time to all the memory words.

* 1. NUMA.
  2. NC-NUMA
  3. UMA
  4. CC-NUMA

1. Many software packages that run on windows are multithreaded. State true or false.
2. True
3. False
4. Interleaved execution of multiple threads in a round-robin fashion occurs in
5. coarse grained multi threading
6. Fine grained multi threading
7. Fine and coarse grained multi threading
8. multi threading
9. has separate data cache and a separate instruction cache.

a)direct-mapped cache b)Dual cache

1. Split cache
2. fully associative cache
3. MESI protocol enforcing data integrity among caches sharing data through
   1. Write back scheme
   2. dirty data
   3. clean data
   4. both (a) and (b)
4. In which mapping, the cache memory has to be very frequently replaced even when other blocks in the cache memory were present as empty?
5. Indirect mapping
6. Fully Associative mapping
7. Set Associative mapping
8. Direct mapping
9. In Set Associative mapping, memory blocks are mapped into following cache set
10. Total no.of sets %memory block number
11. memory block number % Total no.of sets
12. Total no.of sets %cache line number
13. cache line number % Total no.of sets

**Part C**

* 1. Assuming a 15-bit address space with 8 logical pages. How large are the pages?
     1. 2 power 10
     2. 2 power 11
     3. 2 power 12
     4. 2 power 15
  2. Find the hit ratio and miss ratio of the cache when there was 9 hits and 5 misses. a) 14/9 and 14/5

b)14/5 and 14/9

c) 9/14 and 5/14

d) 5/14 and 9/14

* 1. Consider the instructions

A=X1\*X2+X3\*X4

B=X1\*X2-X3\*X4 What is the H/w parallelism average?

a)8/6 b)12/4 c)7/8 d)8/7

* 1. How many tag bits are needed to map 16KB main memory/ to 1KB cache? Consider the word offset to be 4 bits.
     1. 4
     2. 6
     3. 2
     4. 12
  2. Consider the following reference string. Calculate the number of page faults when the page frame size is 4 using LRU policy.

1,2,3,4,2,1,5,6,2,1,2,3,7,6

1. 4
2. 5
3. 14
4. 9

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|  |
| --- |
| C. DMA controller |
| D. All of the above |
| C. Tag bit |
| C. Map of Physical Address and Logical Address |
| C single capacitor and single transistor. |
| A. There are limited number ofpages in an operating system |
| B. Shared memory |
| A. First Position |
| A. single instructions multiple data |
| A. 2^m\* n |
| A. Cache is slower than main memory |
| A. Physical addresses |
| A. Page fault |
| A. Execution |
| C. CUDA thread |
| A. Multiple threads |
| D. All of these |
| A. Modified |
| The memory allocated toeach page is contiguous. |
| C Concurrency |
| B. 222 |
| B. Coarse-grained multi-threading |
| A. Cache coherency overhead |
| D. All of the above |
| C. 8 |
| C. By checking the interrupt register after finishing the execution of the current instruction |
| D. Message Passing Interface |
| B. MESI protocol |
| A. Thread-LevelParallelism |
| B. Output dependence |
| B. Multi-core processor |
| b. Polling |
| D. Instruction Count |
| D. Fully associative |
| D. Translation Buffer |

|  |
| --- |
| D. Both a and b |
| D. Virtual Memory |
| A. NUMA |
| A. Coherence is specified on a per-memory location basis, Consistency is specified with respect to all  memory locations. |
| B. Disable interrupts and priority assignment |
| C. Data and Instruction cache |
| C. Program status word |
| D. All of the above |
| A. LDA |
| C. 16 bits |
| A. Number of bits required for cache indexing = 10, Tag = 17, Line Number =10, Block = 5 |
| C. 2 MB |
| C. 96 ns |
| C. 15 bits |
| A. 110ns |

**Easy Questions**

**Computer Organization and Architecture Unit – IV & V**

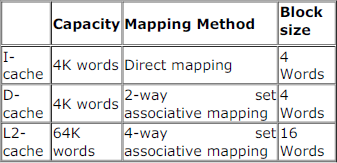
* 1. indicates the concurrency.
     1. Serialization
     2. Parallelism
     3. Serial processing
     4. Distribution
  2. MIPS stand for?
     1. Mandatory Instructions/sec
     2. Millions of Instructions/sec
     3. Most of Instructions/sec
     4. Many Instructions / sec
  3. The Alternative method of a snooping around coherence protocol is known as a
     1. Memory Protocol
     2. Directory Protocol
     3. Register Protocol
     4. None of the above
  4. Private information that is utilized by a single processor and afterward shared information are used by
     1. Single processor
     2. Multi-processor
     3. Single Tasking
     4. Multi-Tasking
  5. The term which is named as shared memory to both Symmetric Multi-Processing and Distributed shared memory alluding that the state address space is
     1. Multi-threading
     2. Recurrence
     3. Dedicated
     4. Shared Memory
  6. At the point when an instruction begins execution and when it closes execution; between these two times the instruction is in
     1. Execution
     2. Wait
     3. Stall
     4. Branching
  7. Combination of instructions, such as compare following a branch and combining them into a one-operation, is taken by
     1. Instruction decode
     2. Instruction fetch
     3. Macro-op fusion
     4. Micro-op fusion
  8. If exploiting and finding the parallelism, across branches require scheduling code, a substantially very difficult algorithm is
     1. Global Scheduling
     2. Local Scheduling
     3. Pre Scheduling
     4. Post Scheduling
  9. SIMD symbolizes an organization that .
     1. refers to a computer system capable of processing several programs at the same time.
     2. represents organization of single computer containing a control unit, processor unit and a memory unit.
     3. **includes many processing units under the supervision of a common control unit.**
     4. None of the above
  10. An option towards the fine-grained multithreading with the conceived procedure was
      1. Buffer-grained multi-threading
      2. Miss-grained multi-threading
      3. Coarse-grained multi-threading
      4. Coarse-grained single threading
  11. To conquer the moderate operating speeds of the secondary memory we utilize quicker and fast flash drives.
      1. True
      2. False
  12. The memory which is utilized to store the duplicate of information or instructions stored in bigger memories, inside the CPU is called
      1. Level 1 cache
      2. Level 2 cache
      3. Registers
      4. TLB
  13. The bigger memory set between the primary cache and the memory is called
      1. Level 1 cache
      2. Level 2 cache
      3. EEPROM
      4. TLB
  14. On the off chance that we utilize the flash drives rather than the hard disks, then the secondary storage can go above primary memory in the hierarchy.
      1. True
      2. False
  15. A small page size will result in less wasted storage when a contiguous region of virtual memory isn't equivalent in size to several of the page size, this unused memory is known as
      1. Segmentation
      2. External fragmentation
      3. Internal fragmentation
      4. All above
  16. The approach for memory hierarchies: L1 information are never found in a L2 store, refers to
      1. Write buffer
      2. Multilevel exclusion
      3. Write-through
      4. Multilevel inclusion
  17. The 64-bit virtual location of the AMD64 architecture is mapped onto
      1. 64 bits physical addresses
      2. 32 bits physical addresses
      3. 52 bits physical addresses
      4. 128 bits physical addresses
  18. The viability of the cache memory depends on the property of
      1. Locality of reference
      2. Memory localization
      3. Memory size
      4. None of the mentioned
  19. The bit used to connote that the cache location is updated is
      1. Dirty bit
      2. Update bit
      3. Reference bit
      4. Flag bit
  20. The methodology where the memory substance are moved directly to the processor from the memory is called
      1. Read-later
      2. Read-through
      3. Early-start
      4. None of the mentioned

**Moderate Questions**

1. Which sort of parallelism utilized for miniature architectural strategies?
   1. Instructional
   2. bit level
   3. bit based
   4. increasing
2. Which is the best adaptable MIMD frameworks regard to the quantity of processors?
   1. Distributed memory computers
   2. ccNUMA systems
   3. nccNUMA systems
   4. Symmetric multiprocessors
   5. None of the answers above is correct
3. is whereinstruction gets stored, while performing a looping operation.
   1. Registers
   2. Cache
   3. System Heap
   4. System stack
4. A Processor (assigned)with a thread block, that executes a code, which we generally call a
   1. Multithreaded DIMS Processor
   2. Multithreaded SIMD Processor
   3. Multithreaded Queue
   4. Multithreaded Stack
5. Each Dependence analysis algorithms operational on the supposition that array indices are
   1. Server
   2. Kernel
   3. Affine
   4. Define
6. Which value hasthe speedup of a parallel program that accomplishes a productivity of 75% on 32 processors?
   1. 18
   2. 24
   3. 16
   4. 20
7. Information or Data level parallelism/task-level parallelism in a firmly coupled equipment which licenses communication among parallel threads, are taken care of by
   1. Instruction-Level Parallelism
   2. Request-Level Parallelism
   3. Thread-Level Parallelism
   4. Vector Architectures and Graphic Processor Units
8. MISD data stream stands for
   1. Multiple instruction single data stream
   2. Multiple instruction streams, single data stream
   3. Multiple instruction streams, data stream
   4. Many instruction streams, single data stream
9. Multiprocessing grants single processor to run a few of synchronous threads.
   1. True
   2. False
10. disclosed as Switch to another thread each cycle with the end goal that has no two directed instructions
    1. Fine-grained multi-threading
    2. Coarse-grained multi-threading
    3. Coarse-grained single threading
    4. Buffer-grained multi-threading
11. To make fine-grained multithreading viable, processor must have the option to switch threads on each .
    1. Process
    2. clock cycle
    3. Instruction stream
    4. Data stream
12. Multithreading on a single processor is conceivable with the assistance of
    1. Threader
    2. Scheduler
    3. Method
    4. Divider
13. Which factor decides the viability of the cache?
    1. hit rate
    2. refresh cycle
    3. refresh rate
    4. refresh time
14. Which of the following is a common cache?
    1. DIMM
    2. SIMM
    3. TLB
    4. Cache
15. What number of possibilities of mapping does a direct mappedcache have?
    1. 1
    2. 2
    3. 3
    4. 4
16. Which of the accompanying refers to the quantity of consecutive bytes which are related with each cache entry?
    1. cache size
    2. associative set
    3. cache line
    4. cache word
17. How much number of divisions is possible in the cache memory dependent on the tag or index address?
    1. 3
    2. 2
    3. 4
    4. 5
18. Critical level or percentage of the spent time in moving information in two levels in the memory hierarchy, then the memory-hierarchy is said to
    1. Thrash
    2. Mixed
    3. Averaging
    4. Write stall
19. On the off chance that each blocks having one place to be show up in the cache, this cache is supposed to be
    1. Indirectly mapped
    2. Directly mapped
    3. Pages
    4. Registers
20. The program is isolated into operable parts called as
    1. Frames
    2. Segments
    3. Pages
    4. Sheets
21. The binary address issued to data or instructions are called as
    1. Physical address
    2. Location
    3. Relocatable address
    4. Logical address
22. Because of virtual memory, the memory can be shared among
    1. Processes
    2. Threads
    3. Instructions
    4. none of the mentioned
23. When a program tries to access a page that is mapped in address space but not loaded in physical memory, then
    1. segmentation fault occurs
    2. fatal error occurs
    3. page fault occurs
    4. no error occurs
24. Which algorithm chooses the page that has not been used for the longest period of time
    1. whenever the page required to be replaced?
    2. first in first out algorithm
    3. additional reference bit algorithm
    4. least recently used algorithm
    5. counting based page replacement algorithm
25. Working set model for page replacement is based on the assumption of
    1. Modularity
    2. Locality
    3. Globalization
    4. random access

**Difficult**

1. A computer system has a level-1 instruction cache (1-cache), a level-1 data cache (D- cache) and a level-2 cache (L2-cache) with the following specifications:



* 1. 1 K x 18-bit, 1 K x 19-bit, 4 K x 16-bit
  2. 1 K x 16-bit, 1 K x 19-bit, 4 K x 18-bit
  3. 1 K x 16-bit, 512 x 18-bit, 1 K x 16-bit
  4. 1 K x 18-bit, 512 x 18-bit, 1 K x 18-bit

1. Consider a computer with a 4-ways set-associative mapped cache of the followingcharacteristics: a total of 1 MB of main memory, a word size of 1 byte, a block size of 128words and a cache size of 8 KB.

The number of bits in the TAG, SET and WORD fields, respectively are: a. 7, 6, 7

b. 8, 5, 7

c. 8, 6, 6

d. 9, 4, 7

1. Intel 8080 microprocessor has an instruction set of 91 instructions. The opcode to implement thisinstruction set should be at least
   1. 3 bit long
   2. 5 bit long
   3. 7 bit long
   4. 9 bit long
2. A cache line is 64 bytes. The main memory has latency 32ns and bandwidth1G.Bytes/s.

The time required to fetch the entire cache line from the main memory is

* 1. 32 ns
  2. 64 ns
  3. 96 ns
  4. 128 ns

1. Consider a machine with a byte addressable main memory of 2bytes. Assume that adirect mapped data cache consistingof 32 lines of 64 bytes each is used in the system. A50 x 50 two-dimensional arrays of bytes is stored in the main memorystarting frommemory location 1100H. Assume that the data cache is initially empty. The complete arrayis accessed twice.Assume that the contents of the data cache do not change in betweenthe two accesses.How many data misses will occur in total?
   1. 48
   2. 50
   3. 56
   4. 59

**CT3: Multiple Choose Questions**

1. buffer ensures the instruction execution sequence and also catches the results.
   1. Ordered buffer

# Reorder buffer

* 1. Data buffer
  2. Control buffer

1. The is the end of instruction execution phase, after which the user gets the final output
   1. Write result
   2. Read result
   3. Execute

# Commit

1. When the data at a location in cache is different from the data located in the main memory, the cache is called

* 1. Unique

# Inconsistent

* 1. Variable
  2. Fault

1. Categorize the way in which the performance is increased with pipelining
   1. By decreasing instruction latency
   2. By eliminating data hazards

# By exploiting instruction level parallelism

* 1. By decreasing the cache miss rate

1. When a page is selected for replacement, and its modify bit is set :
   1. The page is clean
   2. The page has not been modified since it was read in from the disk

# The page is dirty

* 1. The page is currently used

1. To exploit the objective of S/W and H/W techniques, used.

# Parallelism

* 1. Scalability
  2. Supervision
  3. Compatibility

1. OS maintains the page table for .
   1. Each data element
   2. Each instruction
   3. Each address

# Each process

1. is used for Run time mapping from virtual to physical address.

# Memory Management Unit

* 1. CPU
  2. PCI
  3. Cache

1. is used in local memory to multithreaded the Single Instruction Multiple data (SIMD) processor.
   1. Global Memory

# On\_chip Memory

* 1. Flash Memory
  2. Stack

1. The amount of time required to read a block of data from a disk into memory is composed of seek time, rotational latency, and transfer time. Rotational latencyrefers to .

# The time it takes for the platter to make a full rotation

* 1. The time it takes for the read-write head to move into position over the appropriate track
  2. The time it takes for the platter to rotate the correct sector under the head
  3. It takes for sector reading

1. The cache memory exploits the property of programs.

# Principle of locality

* 1. on the heuristic 90-10 rule
  2. on the fact that references generally tend to be farther
  3. page replacement

1. The processor is called to execute a code when a processor experiences a thread block.
   1. Multithreaded DIMS

# Multithreaded SIMD

* 1. Multithreaded Queue
  2. Multithreaded Stack

1. is the average time required to reach a storage location in memory and obtain its contents.
   1. Latency time

# Access time

* 1. Turnaround time
  2. Response time

1. If the access time of a cache is 1nS, and the access time of a main memory is 15nS, assuming that the Cache hit rate is 0.9 and the total number of accesses are 100; then the average access times of the access with cache and without cache will be and .

# 250 nS and 1500 nS

* 1. 250mS and 150 nS
  2. 25 nS and 1500nS
  3. 250mS and 1500mS

1. To overcome the conflict over the possession of the BUS used.
   1. Optimizers

# BUS arbitrators

* 1. Multiple BUS structure
  2. None of the mentioned

1. DMA interface unit eliminates the need to use CPU registers to transfer data from
   1. MAR to MBR
   2. MBR to MAR
   3. I/O units to memory

# Memory to I/O units

1. is the values of speedup of a parallel program that achieves only 75% efficiency on 32processors?
   1. 18

# 24

* 1. 16
  2. 20

1. Which MIMD frameworks are best adaptable with respect to the quantityof processors?

# Distributed memory computers

* 1. ccNUMA systems
  2. nccNUMA systems
  3. Symmetric multiprocessors

1. Which Flynn’s classification belongs to von Neumann computer
   1. SIMD (Single Instruction Multiple Data)
   2. MIMD (Multiple Instruction Multiple Data)
   3. MISD (Multiple Instruction Single Data)

# SISD (Single Instruction Single Data)

1. When the organization includes many processing units under the supervision of a common control unit, is used.

# SIMD (Single Instruction Multiple Data)

* 1. MIMD (Multiple Instruction Multiple Data)
  2. MISD (Multiple Instruction Single Data)
  3. SISD (Single Instruction Single Data)

1. To build 1M Byte memory, how many RAM chips of size (256K x 1 bit) are required?

* 1. 8

* 1. 12
  2. 24

# 32

1. The information when is written in the cache, both to the block in the cache and the block present in the lower-level memory, refers to

* 1. Miss rate

* 1. Write-back

# Write-through

* 1. Dirty bit

1. Which of the following is the fastest means of memory access for CPU?

# Registers

* 1. Cache

* 1. Main memory

* 1. Virtual Memory

1. Transfer of data directly between a peripheral and memory without the aid of CPU is achieved using

* 1. NMI controller

* 1. DDR controller

# DMA controller

* 1. Interrupt controller

1. Block Transfer from memory will be beneficial due to which of the following?

* 1. Spatial Locality

* 1. Lesser Memory Latency

* 1. Paging

# Paging,Memory Latency and Spatial Locality

1. The Translation Look Aside Buffer (TLB) stores

* 1. Branching data

* 1. Map of Cache data and RAM data

# Map of Physical Address and Logical Address

* 1. Memory Translation times

1. A single DRAM memory cell contains

* 1. Single capacitor and multiple transistors.

* 1. Multiple capacitors and single transistor.

# Single capacitor and single transistor.

* 1. Multiple capacitors and multiple transistors.

1. Consider the data bus width of DDR memory system is 32 bits. How many cycles does it take to transfer 64B cache block?

* 1. 64

* 1. 16

# 8

* 1. 1

1. A CPU generally handles an interrupt by executing an interrupt service routine

* 1. As soon as an interrupt is raised

* 1. By checking the interrupt register at the end of fetch cycle

# By checking the interrupt register after finishing the execution of the current instruction

* 1. By checking the interrupt register at fixed intervals.

1. What is its total capacity, when a hard disk with 5 platters has 2048 tracks/platter, 1024 sectors/track (fixed number of sectors per track), and 512-bytesectors?

* 1. 7GB

# 5GB

* 1. 4GB

* 1. 8GB

1. Which among the following is true?

# The memory allocated to each page is contiguous.

* 1. The offset is different in a virtual address and a physical address

* 1. Logical address space can be smaller than physical address space

* 1. Segmentation avoids external memory fragmentation

1. When the data can be mapped anywhere in the cache memory, which type of mapping can be used?

# Associative

* 1. Direct

* 1. Set Associative

* 1. Indirect

1. Which category the Single instruction single data stream (SISD) belongs to?

# Uniprocessor category

* 1. Dual Processor category
  2. Quad core category
  3. Multiple processor

1. MISD data stream stands for
   1. Multiple Instruction Single Data stream

# Multiple Instruction streams, Single Data stream

* 1. Multiple Instruction streams, Data stream
  2. Many Instruction streams, Single Data stream

1. helps to execute the multiple tasks independently.
   1. Multithreading

# Multiprogramming

* 1. Multitasking
  2. Synchronization

1. and are the streams act either as a serial or parallel.

# Data stream and Task stream.

* 1. Instruction stream and program stream.
  2. Program stream and bit stream.
  3. Data stream and synchronization stream.

1. Task parallelism is meant as the?

# Way to parallelize a program by making different processors executes different programs.

* 1. Way to parallelize a program by making different processors executes the same program on different sets of data.
  2. Way to parallelize a program by making it rerun once it is finished.
  3. Way to make a program to help other programs when they have a lot of work to do.

1. The array processor has
   1. Different memory

# Local memory

* 1. Two memory
  2. All of the above

1. is used to configure the MIMD.

# A multiprocessor

* 1. A vector processor
  2. Array processor
  3. None of the above.

1. The vectored interrupt is
   1. The branch address is assigned to a fixed location in memory

# The interrupting source supplies the branch information to the processor through an interrupt vector

* 1. The branch address is obtained from a register in the processor
  2. None of the mentioned

1. Where the instructions get stored, While performing a looping operations, instructions are stored in .
   1. Registers

# Cache

* 1. System Heap
  2. System stack

1. SIMD signifies an association that .
   1. Refers to a computer system capable of processing several programs at the same time
   2. Represents organization of single computer containing a control unit, processor unit and a memory unit

# Includes many processing units under the supervision of a common control unit

* 1. Single processing units under the supervision of a common control unit

1. The multithreading is also known as
   1. Simultaneity
   2. Crosscurrent

# Concurrency

* 1. Recurrent

1. described as Switch to another thread every cycle such that no two instructions from the similar thread are in the pipeline at the same time.

# Fine-grained multi-threading

* 1. Coarse-grained multi-threading
  2. Coarse-grained single threading
  3. Buffer-grained multi-threading

1. A computer has an 8 GB memory with 64 bit word sizes. Each block of memory stores 16 words. The computer has a direct-mapped cache of 128 blocks. The computer uses word level addressing. What is the address format?

a. 19 – 7 – 4

b. 18 – 7 – 5

c. 19 – 6 – 5

d. 18 – 6 – 6

1. A block-set associative cache memory consists of 128 blocks divided into four block sets. The main memory consists of 16,384 blocks and each block contains 256 eight bit words. How many bits are required for addressing the main memory?
   1. 20
   2. 22
   3. 23
   4. 19
2. A block-set associative cache memory consists of 128 blocks divided into four block sets. The main memory consists of 16,384 blocks and each block contains 256 eight bit words. How many bits are needed to represent the TAG, SET and WORD fields?

a. 9-5-8

b. 5-8-9

c. 8-9-5

d. 19-6-7

1. A system uses 3 page frames for storing process pages in main memory. It uses the First in First out (FIFO) page replacement policy. Assume that all the page frames are initially empty. What is the total number of page faults that will occur while processing the page reference string 60, 12, 7, 6, 3, 7, 6, 3, 2, 7?
   1. 6
   2. 8
   3. 7
   4. 5
2. A system uses 4 page frames for storing process pages in main memory. It uses the First in First out (FIFO) page replacement policy. Assume that all the page frames are initially empty. What is hit ratio and miss ratio that will occur while processing the page reference string 50, 4, 7, 6, 1, 7, 6, 1, 2, 7?

a. 60%: 40%

b. 40%: 60%

c. 50%:50%

d. 30%:70%

1. A system uses 3 page frames for storing process pages in main memory. It uses the Least Recently Used (LRU) page replacement policy. Assume that all the page frames are initially empty. What is the total number of page faults that will occur while processing the page reference string 8 , 9, 5, 4, 9, 5, 4, 2, 8, 2.
   1. 7
   2. 5
   3. 6
   4. 4

# Unit –IV MCQ

1. Name the buffer which ensures the instruction execution sequence and also catches the results
   1. Ordered buffer

# Reorder buffer

* 1. Data buffer
  2. Control buffer

1. The is the end of instruction execution phase, after which the user gets the final output
   1. Write result
   2. Read result
   3. Execute

# Commit

1. Identify the way in which the performance is increased with pipelining
   1. By decreasing instruction latency
   2. By eliminating data hazards

# By exploiting instruction level parallelism

* 1. By decreasing the cache miss rate

1. The objective of S/W and H/W techniques, is to exploit

# Parallelism

* 1. Scalability
  2. Supervision
  3. Compatibility

1. The local memory to multithreaded Single Instruction Multiple data (SIMD) processor is a
   1. Global Memory

# On\_chip Memory

* 1. Flash memory
  2. Stack

1. The is called to execute a code when a processor experiences a thread block
   1. Multithreaded DIMS Processor

# Multithreaded SIMD Processor

* 1. Multithreaded Queue
  2. Multithreaded Stack

1. The is the ’unifying theme’ of every forms of parallelism in NVIDIA
   1. CDA thread
   2. PTA thread

# CUDA thread

* 1. CUD thread

1. The is the instruction created by hardware machine object for managing, scheduling and executing
   1. DIMS instructions
   2. DMM instructions

# SIMD instructions

* 1. SIM instructions

1. When instruction i and instruction j are tends to write the same register or the memory location, it is called
   1. Input dependence

# Output dependence

* 1. Ideal pipeline
  2. Digital call

1. The instruction is said to be in while it is between it’s start and end of its running phase.

# Execution

* 1. Wait
  2. Stall
  3. Branching

1. The algorithm is difficult for exploiting and finding the parallelism between branches and scheduling

# Global Scheduling

* 1. Local Scheduling
  2. Pre Scheduling
  3. Post Scheduling

1. The do not have parallel processing capabilities

# Single Instruction stream, Single Data stream

* 1. Single Instruction stream, Multiple Data stream
  2. Multiple Instruction stream, Multiple Data stream
  3. All of the above

1. is the values of speedup of a parallel program that achieves only 75% efficiency on 32 processors?
   1. 18

# 24

* 1. 16
  2. 20

1. Parallel programs: Which speedup could be achieved according to Amdahl´s law for infinite number of processors if 5% of a program is sequential and the remaining part is ideally parallel?
   1. Infinite speedup
   2. 5

# 20

* 1. 50

1. Which MIMD frameworks are best adaptable with respect to the quantity of processors?

# Distributed memory computers

* 1. ccNUMA systems
  2. nccNUMA systems
  3. Symmetric multiprocessors

1. which class of systems belongs to von Neumann computer
   1. SIMD (Single Instruction Multiple Data)
   2. MIMD (Multiple Instruction Multiple Data)
   3. MISD (Multiple Instruction Single Data)

# SISD (Single Instruction Single Data)

1. SIMD symbolizes an organization that .
   1. refers to a computer system capable of processing several programs at the same time.
   2. represents organization of single computer containing a control unit, processor unit and a memory unit.

# includes many processing units under the supervision of a common control unit.

* 1. none of the above

1. Types of parallelism in the applications are
   1. Data-Level Parallelism
   2. Task-Level Parallelism
   3. Instruction-Level Parallelism

# All above

1. Single instruction single data stream (SISD) category is the

# Uniprocessor category

* 1. Dual Processor category
  2. Quadcore category
  3. Multiple processor

1. Data-level parallelism/task-level parallelism in a tightly coupled equipment which permits communication among parallel threads, are handled by
   1. Instruction-Level Parallelism
   2. Request-Level Parallelism

# Thread-Level Parallelism

* 1. Vector Architectures and Graphic Processor Units

1. Single instruction single data stream (SISD) category is the

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1. Data-level parallelism/task-level parallelism in a tightly coupled equipment which permits communication among parallel threads, are handled by
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# Thread-Level Parallelism

1. Vector Architectures and Graphic Processor Units
2. MISD data stream stands for
   1. Multiple instruction single data stream

# Multiple instruction streams, single data stream

* 1. Multiple instruction streams, data stream
  2. Many instruction streams, single data stream

1. Multiprocessing permits single processor to run a few simultaneous threads.

# True

* 1. False

1. Multiple tasks executing independently is called as
   1. Multithreading

# Multiprogramming

* 1. Multitasking
  2. Synchronization

1. The and are the streams from Flynn's taxonomy which can be either be a serial or parallel
   1. **Data stream and task stream.**
   2. Instruction stream and program stream.
   3. Program stream and bit stream.
   4. Data stream and synchronization stream.
2. What do you mean by task parallelism?
   1. **It is a way to parallelize a program by making different processors executes different programs.**
   2. It is a way to parallelize a program by making different processors executes the same program on different sets of data.
   3. It is a way to parallelize a program by making it rerun once it is finished.
   4. It is a way to make a program to help other programs when they have a lot of work to do.
3. Generally the array processor has
   1. Different memory

# Local memory

* 1. Two memory
  2. All of the above

1. MIMD configuration can be called as

# A multiprocessor

* 1. A vector processor
  2. Array processor
  3. None of the above.

1. The multiplier -6(11010) is detailed as

# a. 0-1-2

b. 0-1+1-10

c. -2-10

d. none of the mentioned

1. Using technique the summands can be decreased to half
   1. Fast multiplication

# Bit-pair recording

* 1. Quick multiplication
  2. None of the mentioned

1. Which is the suitable one for increasing processor word size in a parallelism.
   1. Increasing
   2. Count based
   3. Bit based

# Bit level

1. Which type of parallelism used for micro architectural techniques?

# Instructional

* 1. bit level
  2. bit based
  3. increasing

1. Computer system of a parallel computer is capable of

# Decentralized computing

* 1. Parallel computing
  2. Centralized computing
  3. Distributed computing

1. Scripting parallel programs is termed as
   1. Parallel computation
   2. Parallel processes
   3. Parallel development

# Parallel programming

1. At what time the parallel processing will occur?
   1. in the instruction stream
   2. in the data stream

# both [A] and [B]

* 1. none of the above

1. The cost of a parallel processing can be resolute by
   1. Time Complexity
   2. Switching Complexity

# Circuit Complexity

* 1. None of the above

1. Which is the best scalable MIMD systems respect to the number of processors?

# Distributed memory computers

* 1. ccNUMA systems
  2. nccNUMA systems
  3. Symmetric multiprocessors
  4. None of the answers above is correct

1. In a vectored interrupt
   1. The branch address is assigned to a fixed location in memory

# The interrupting source supplies the branch information to the processor through an interrupt vector

* 1. The branch address is obtained from a register in the processor
  2. None of the mentioned

1. Where the instructions gets stored, while performing a looping operations.
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# Cache

* 1. System Heap
  2. System stack

1. SIMD signifies an association that .
   1. refers to a computer system capable of processing several programs at the same time
   2. represents organization of single computer containing a control unit, processor unit and a memory unit

# includes many processing units under the supervision of a common control unit

* 1. single processing units under the supervision of a common control unit

1. The is the another name given to multithreading
   1. Simultaneity
   2. Crosscurrent

# Concurrency

* 1. Recurrent

1. Multiprocessing permits uni processor to route numerous simultaneous threads.

1. True

# False

1. An is a best replacement for fine grained multithreading
   1. Buffer-grained multi-threading
   2. Miss-grained multi-threading

# Coarse-grained multi-threading

* 1. Coarse-grained single threading

1. An instruction stream is arrangement of instructions performed by machine

# True

* 1. False

1. Flynn's Classification discriminates multi-processor computer structural design rendering to

# Independent dimensions of Instruction stream and Data stream

* 1. Dependent dimensions of Instruction stream and data stream.
  2. Independent dimensions of memory and processor.
  3. Dependent dimensions of memory and I/O stream.

1. described as Switch to another thread every cycle such that no two instructions from the similar thread are in the pipeline at the same time.

# Fine-grained multi-threading

* 1. Coarse-grained multi-threading
  2. Coarse-grained single threading
  3. Buffer-grained multi-threading

1. Hardware multithreading permits several threads to share functional units of a in an overlying manner.

# Single processor

* 1. Multi-processor
  2. multithreading
  3. Single threading

1. Fine-grained multithreading changes amongst threads on each instruction, causing in interweaved accomplishment of .

# Multiple threads

* 1. Single threads
  2. Multicore process
  3. Single process

1. Coarse-grained multithreading shifts threads only on expensive stands, alike former level

.

* 1. Instruction stream

# cache misses

* 1. multi process
  2. shared memory

1. To sort fine-grained multithreading hands-on, processor need to be capable in shifting threads on each .
   1. Process

# clock cycle

* 1. Instruction stream
  2. Data stream

1. Using Multithreading can be implemented on single processor
   1. Threader

# Scheduler

* 1. Method
  2. Divider

1. Scheduler shift threads in
   1. Multilevel queue scheduling
   2. Priority Scheduling

# Round robin fashion

* 1. Multilevel feedback queue scheduling

1. sorts it conceivable for greater than equal to dual accomplishments to effect in parallel on a single processor.

# Multithreading

* 1. Threading
  2. Single Threading
  3. Both Multithreading and Single Threading

1. Cache Coherence Problem ensues with respect to
   1. Sharing of writable data.
   2. Process migration.
   3. Inconsistency due to I/O

# All of these

1. A outfits multiprocessing in a sole physical suite.
   1. Multithreading

# Multi-core processor

* 1. Multiprocessor
  2. Parallel processor

1. Enactment of the Multicore processor is independent of
   1. Frequency
   2. Number of cores
   3. Program to be executed

# Clock frequency of the core

1. MESI Protocol is a sort of inquisitive

# Cache protocol

* 1. Processor protocol
  2. Memory protocol
  3. Instruction protocol

1. In MESI Protocol, state specifies that the cache line is existing in current

cache only and its significance is diverse from the main memory.

# Modified

* 1. Exclusive
  2. Shared
  3. Invalid

1. A hands-on multiprocessor undermine protocol which efforts to diminish bus procedure is



* 1. MOESI protocol

# MESI protocol

* 1. MSI protocol
  2. MOSI protocol

1. In MESI protocol, Incident may be owing to

# Either local processor activity or bus activity

* 1. Only local processor activity
  2. Only bus activity
  3. Neither local processor activity nor bus activity

1. ensures write back caches.
   1. MOSI protocol
   2. MOESI protocol

# MESI protocol

* 1. MSI protocol

1. A write is only performed liberally in MESI protocol, if the cache line is in

# Either Modified or Exclusive state

* 1. Modified state only
  2. Shared state or Invalid state
  3. Shard state only

1. denotes the accomplishment of several software practice simultaneously.
   1. Serial communication

# Multiprocessor

* 1. DCP
  2. IOP

1. expands the trustworthiness of the system so that a letdown or fault in single portion has a partial result on the other portions.
   1. Uniprocessing
   2. Multicore processing
   3. Parallel processing

# Multiprocessing

1. A multithreaded CPU is not a parallel architecture

# True

* 1. False

1. More number of clock cycles is wasted in \_
   1. Fine-grained multi-threading

# Coarse-grained multi-threading

* 1. Coarse-grained single threading
  2. Buffer-grained multi-threading

1. utilizes less amount of computational time.

# Fine-grained multi-threading

* 1. Coarse-grained multi-threading
  2. Coarse-grained single threading
  3. Buffer-grained multi-threading

1. In , high level of parallelism is available.
   1. Fine grained SIMD
   2. Coarse grained SIMD
   3. Fine grained SISD
   4. Fine grained MISD
2. Multithreading uses to improve utilization of a single processor.
   1. thread-level parallelism
   2. core level parallelism
   3. SIMD
   4. SISD
3. is a full cache coherence protocol that encompasses all of the possible states commonly used in other protocols.
   1. MOESI protocol

# MESI protocol

* 1. MSI protocol
  2. MOSI protocol

1. Memory management on a multiprocessor must deal with all of found on

# Uniprocessor system

* 1. Parallel system
  2. Pipeline
  3. Threads

1. is an extension of MSI protocol
   1. MOESI protocol
   2. MESI protocol

# MOSI protocol

* 1. All of these

1. A cache line in state does not hold a valid copy of data with respect to MOESI protocol.
   1. Shared
   2. Exclusive

# Invalid

* 1. Owned

1. In **MOESI Protocol**, A cache line in state holds the most recent, correct copy of the data but copy in main memory can be incorrect.
   1. Shared
   2. Exclusive
   3. Invalid

# Owned

1. Most commonly used cache coherence protocol is
   1. MOESI protocol

# MESI protocol

* 1. MSI protocol
  2. MOSI protocol

1. has all the five states present in it.
   1. MOESI protocol

# MESI protocol

* 1. MSI protocol
  2. MOSI protocol

1. When a processor needs to read a block which none of the other processors have and then write to it, the MESI protocol uses .
   1. Shared

# Exclusive

* 1. Invalid
  2. Owned

1. In computer architecture, is the uniformity of shared resource data that ends up stored in multiple local caches.

# cache coherence

* 1. thread level parallelism
  2. multicore processor
  3. unicore processor

1. MESI cache coherence protocol ensures for processors with caches.
   1. Sequential Consistency
   2. Parallel Consistency
   3. Sequential coherence
   4. Exclusive consistency
2. Which memory unit is used for reducing the access time from memory?
   1. DRAM
   2. SRAM
   3. Cache
   4. Secondary Answer: C
3. In Load R1,LOCA. Add R0, R1. Contents that would be overwritten are :
   1. R0
   2. R1
   3. LOCA
   4. R0 and R1 Answer: A
4. 1 Megabytes is equal to a. 220

b. 210

c. 230

d. 240

Answer: A

1. 32MB of memory in a computer would require how many bits to address any single byte in a memory
2. 25 bits
3. 32 bits
4. 24 bits
5. 25 bytes Answer: A
6. In Big Endian format, of 64 bit data, what is the starting byte address of the aligned words? a. 0,8,16

b. 0,2,4

c. 0,4,8

d. 2,4,6

Answer: A

1. Which instruction is used to move the data to top of the stack?
   1. PUSH A
   2. POP B
   3. PUSH AX
   4. POP Answer: A
2. considering when the value of a number exceeds the range specified by the size of bit field, Which bit in status flag is updated?
3. Negative
4. Carry
5. Zero
6. Overflow Answer: B
7. When adding 0 1 1 1 0 0 1 1 and 1 1 1 0 1 1 0 0, as a result what will be values of the status flag? a. Z=0, c=1,s=0, v=0

b. Z=1,c=0,s=0,v=0

c. Z=0, c=1, s=0, v=1

d. Z=0,c=0,s=0,v=1

Answer: A

1. Which is an example of auto decrement mode addressing? a. Add 1000(R1),R2
2. Add -(R3),R2
3. Add (R3)-,R2
4. SUB (A)+,R2 Answer: B
5. In which type of addressing there is no memory related operation?
6. Register indirect addressing
7. Register addressing
8. Direct addressing
9. Indirect addressing Answer: B

11.If AX=10001001

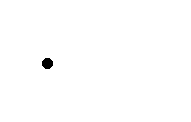
SHL AX,01 what will be output? a. 00010010

b. 00010011

c. 10001001

d. 00010000

Answer: A

1. Which instruction is used for moving the data from accumulator to memory?
2. LOAD D
3. STORE C
4. ADD D
5. MOVE D Answer: B
6. How many one address instructions are needed for evaluating (A+B) (C+D)?
7. 3
8. 7
9. 6
10. 5 Answer: B
11. When you do division operation on two 16 bits numbers in 8086 microprocessor, which of the following registers are used to store the quotient and remainder?
12. AX and DX
13. AX and BX
14. AX and CX
15. BX and DX Answer: A
16. Which of the following segment is used for string operation and storing extra bit of data
17. Code Segment
18. Data Segment
19. Extra Segment
20. Stack segment Answer: C
21. Which of the following registers are used for performing count operation in 8086
22. BX
23. AX
24. CX
25. DX Answer: C
26. SUM EQU 200 does the following
    1. 200 value is assigned after the first occurrence of sum
    2. Value 200 is replaced with every occurrence of sum
    3. Address of Sum is reassigned by adding 200 to original address
    4. 200 bytes of memory is assigned starting from the location of sum Answer: B
27. What is the operation of the instruction MOVE (PC),(MAR)?
28. Move the contents from MAR to PC
29. Move the address from MAR to PC
30. Move the contents of PC to MAR
31. Move the data from Ro to PC to MAR Answer: C
32. You are given the following instruction: ADD AX , [2024]

You are provided the following data:

DS = 3400H ; SS = 1200H ; CS= 4000H

Find the effective address location for the given instruction. a. 36024 H

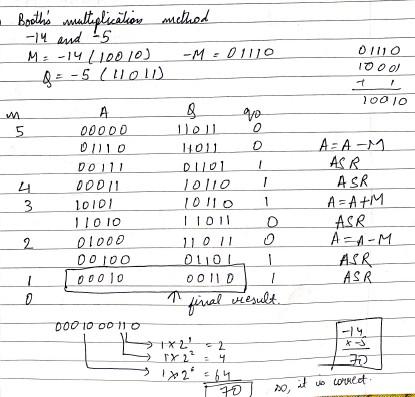
b. 14024 H

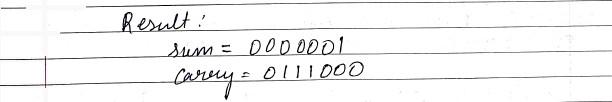
c. 42024 H

d. 44470 H

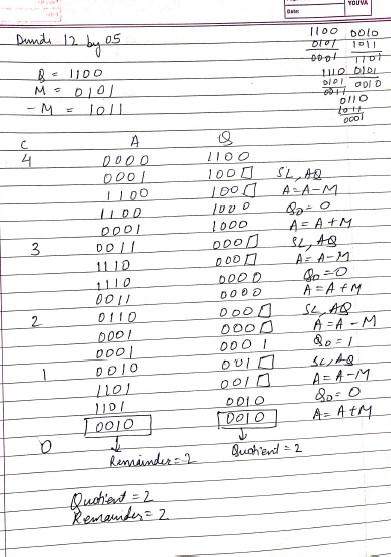
Answer: A

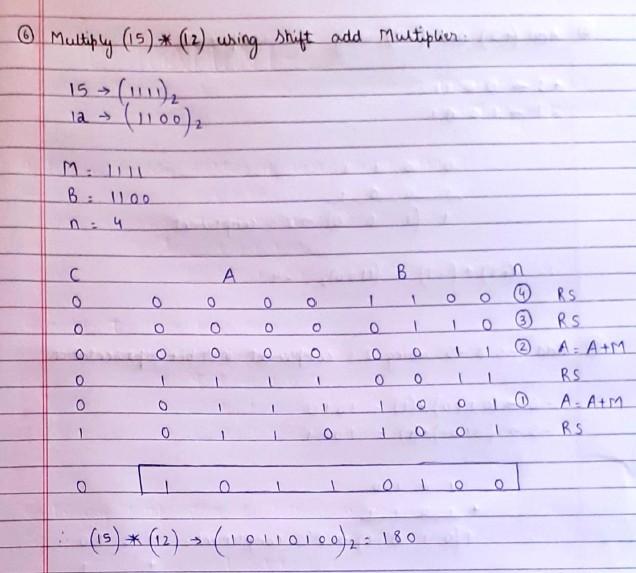
1. Which addressing mode is being used in the given instruction? MOV AX, [1234H]
2. Base Addressing Mode
3. Immediate Addressing Mode
4. Register Addressing Mode
5. Direct Addressing Mode Answer: D
6. INC AX instruction increments the AX register contents by
7. 2
8. 1
9. 4
10. 8 Answer: B
11. When the ARM processor running in thumb state, what will be the size of the instructions?
12. 16
13. 6
14. 32
15. 24 Answer: A
16. How many registers ARM processor possess?
17. 37
18. 42
19. 30
20. 28 Answer: A
21. Each instruction in ARM are encoded into how many words
22. 2 bytes
23. 4 bytes
24. 8 bytes
25. 3 byte Answer: B
26. A DB 30 DUP (‘HI’), how many bytes of memory are defined and reserved by this instruction?
27. 60
28. 30
29. 40
30. 32 Answer: A





1 *0* I D





# SRM Institute of Science and Technology Department of Computer Science and Engineering

**Subject Title: Computer Organization and Architecture Subject code: 18CSC203J**

**CT2Questions Date: 19.10.2020 Time: 9.00 a.m. to 10.30 a.m.**

**MARKS (50) SECTION A (EASY)(20\*1=20)**

1.

When adding two signed n-bit numbers, the signal is ignored from MSB position.

1. carry out
2. carry in
3. positive
4. Negative ANSWER: A 2

.………….. reduces the number of summands by a factor of 2.

1. Bit pair recoding
2. Binary pair recoding
3. Singe bit recoding
4. Multiple pair recoding ANSWER: A

3.

The representation of numbers occupies a large amount of memory.

1. 1’s complement
2. 2’s complement
3. signed numbers
4. Signed magnitude

ANSWER: D 4

A nibble is a group of ……. bits

1. 16
2. 8
3. 4
4. 2 ANSWER: C

5.

In sequential binary multipliercircuit,multiplier bit is stored in .

1. A register
2. Shift register
3. M register
4. n-bit adder ANSWER: B

6

. ………is/are used to implement the sum circuit using full adders.

1. AND & OR Gates
2. NAND gate
3. XOR
4. XNOR ANSWER: C 7

. …………… is used in decimal numbers when a value is written to the power of 10.

1. Height factors
2. Size factors
3. Scale factors
4. Form Factors ANSWER: C

8.

The multiplication is implemented using ……….

1. Flip flops
2. Combinatorial
3. Fast adders
4. Full adders ANSWER: C

9.

Value represented in single precision is \_. A.+/- 1.M \*2^E’-127

B.+ 1.M\*2^E’-126

C. + 1.M\*2^E’-125

D. - 1.M\*2^E’-127

Answer: A

10.

is the size of mantissa in Double Precision IEEE standard floating-point format. A.10-bit

B.11-bit C.23-bit D.52-bit Answer:D

11.

The instruction fetch unit has executed branch instruction concurrently with execution of other instruction is termed as

1. Branch folding
2. Prediction
3. Delayed branching
4. Static prediction Answer: A

12.

The conditional branch instruction outcome can be predicted before the execution by using a logic called

1. Branch prediction
2. Delayed branch C.Structural hazard D.Static prediction Answer: A

13.

Y, temp and Z in single bus organization refers to

* 1. General purpose registers used by the processor
  2. Temporary registers used by processor
  3. Accumulator
  4. Special purpose registers used by processor Answer: B

14.

Prediction decision may change depending on the execution history is

1. Static prediction
2. Dynamic prediction
3. Branch instruction
4. Penalty Answer: **B**

15.

A technique which is used to minimize the penalty caused by conditional branch is



1. Delayed branching
2. Branch penalty
3. Delay
4. Prediction Answer: A

16.

Operand forwarding method doesthe following to overcome data dependencies

1. Introduce NULL instructions
2. Result of the instruction is written to the temporary register
3. Result of one instruction is directly sent to the next instruction for execution
4. Blocking the execution of instructions Answer: C

17.

When the control signal RUN is set to 1 in hardwired control systems

1. The counter is to be incremented by 1 at the end of every clock cycle
2. The counter is to be incremented by 2 at the end of every clock cycle
3. The counter is to be incremented by 3 at the end of every clock cycle
4. The counter is to be incremented by 4 at the end of every clock cycle Answer: A

18.

Which addressing mode is capable of working without fetch operation?

1. Register indirect
2. Direct
3. Indexed
4. Immediate

Answer: D 19.

Which of the following cannot be a condition code?

1. Overflow
2. Zero result
3. Positive result
4. Negative result

# Answer: c

20.

Which of the following statement is true with respect to the function of WMFC signal?

1. Used to make processor wait for the reply from memory
2. Execution of memory instructions
3. Idle state of memory
4. No operation Answer: A

# Section B (MEDIUM)( 15\*1=15)

1.

In binary division, A and Q registers are shifted by .

1. right one binary position
2. left one binary position
3. left two binary positions
4. right two binary positions ANSWER: B

2.

The sum of the two binary numbers, 0110 & 0110 is …….

A. 1100

B. 1111

C. 1001

D. 1010 ANSWER: A 3.

The function*ci + 1 = yici + xici + xiyi*is a carry generation implemented in .

1. Half adders
2. Full adders
3. Ripple adders
4. Fast adders ANSWER: B

4.

Multiplier bit-pair recoding table, under which condition multiplicand selected at Position i is -2\*M.

A. 1 0 1

B. 1 0 0

C. 0 1 1

D. 1 1 0

Answer: B

5.

…….. is the recoding of the multiplier -6(11010) A. 0-1-2

B. 0-1+1-10

C. -2-10

D. 0+1-1-10 ANSWER: A

6.

Innon-restoring division algorithm, for Dividend=1000 and Divisor=100. How many cycles are required to get the correct division result?

A.4

B.5

C.3

D.6

Answer:A 7.

What is the relation between sign exponent E and bias exponent E’ in single precision floating point number?

A.E=E’-1023 B.E=E’+127 C.E=127-E’ D.E=E’-127

Answer:A

8.

The relation between the performance of the pipeline and the no. of stages used in the pipeline are

* 1. Directly proportional
  2. Inversely proportional
  3. No relation between them
  4. None

# Answer: a

9.

What is the reason for incrementing the PC by 4 in multi-bus organization?

1. The word size is 8 bit
2. The word size is 16 bit
3. The word size is 32 bit
4. The word size is 64 bit

# Answer: C

**10.**

The function of Rin is to

1. load the data from bus to register
2. place the content of register onto the bus
3. fetch the data
4. execute the data Answer: A

11.

Add #X, R1, R2. This instruction performs the operation A. R1<- X+[R2]

B. R1->X+[R2]

C. R2<-X+[R1]+[R2]

D. R2<-X+[R1]

Ans : d) R2<-X+[R1]

# 12.



**.**

The above sequence of opertations represents

1. R3=R1+R2
2. R1=R2+R3
3. R2=R1+R3
4. R3=R2-R1

Answer: A

13.

Which expression gives the offset value?

1. Offset= (address immediately following the branch instruction)-(branch target address )
2. Offset=address immediately following the branch instruction-(PC)
3. Offset=(PC)-(address immediately following the branch instruction)
4. Offset= (branch target address) – (address immediately following the branch instruction.)

# Answer: D

14.

How many buffers are required in the Hardware organization for 2 stage pipeline and4 stage pipeline?

A. 2, 1

B. 1, 3

C. 3, 1

D. 2, 4

Answer: B

# 15.

If the state machine moves from LNT to LT in two stage algorithm then

1. branch is taken
2. branch is not taken
3. branch is strongly taken
4. branch is strongly not taken Answer: A

# Section C DIFFICULT (5\*1=5)

1.

What is the result of IEEE double precision representation for (1259.125)?

A.0100000010010011101011001....

B.1100000010010011101011001....

C.1111000010010011101011001....

D.0100001110010011101011001....

Answer: A

2.

Innon-restoring division algorithm, after performing left shift operation on A, Q registers, if magnitude of A < 0 then?

A.Q0=0, A=A+M B.A=A+M C.Q0=1

* 1. =A-M

Answer: B

3

. …….. is the Booth recoded multiplier bit of the multiplier 11010

A. 0 -1 -1 0 0

B. 0 -1 +1 +1 0

C. 0 -1 +1 -1 0

D. 0 +1 -1 -1 0 ANSWER: C 4.

Let there be two instructions I1 and I2 such that: I1 : ADD R1, R2, R3

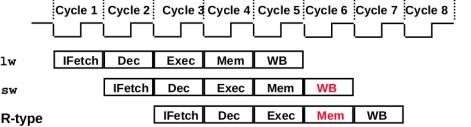
I2 : SUB R4, R1, R2

Identify the type of hazard which occurs in the above instruction

* + 1. Structural hazard
    2. Data hazard
    3. Control hazard
    4. Instructional hazard Answer: Data hazard

5.

Consider the sequence of three MIPS instructions being executed by a pipelined processor as depicted on the figure below. What is the CPI (Clock cycles per instruction) of this sequence?



A. 7/3

B. 6/3

C. 4/3

D. 9/3

Answer: A

# PROBLEMS (Answer any two)

**Section D-(2\*5=10)**

**(NOTE: SECTION D: -You should write answer in A4 sheets, scan your answers and save it as a single PDF file withfilename:your Register Number)**

1. Compute the Multiplicationof (-14) and (-5) using Booths Algorithm (5 marks)
2. Carry out themultiplication of (15) and (12) using shift add multiplier (5 marks)
3. Divide 12 by 5 using non restoring division methods (5 marks)
4. Perform Carry Save Addition for the following numbers 1001,1101,1110,1111,1010,1100. Compute sum and carry as result. (5 Marks)
   1. register Connected to the Processor bus is a single-way transfer capable.
      1. PC
      2. IR
      3. Temp
      4. Z Ans:D
   2. The addressing mode which makes use of in-direction pointers is
      1. Indirect addressing mode
      2. Index addressing mode
      3. Relative addressing mode
      4. Offset addressing mode Ans:A
   3. In the following indexed addressing mode instruction, MOV 5(R1), LOC the effective address is
      1. EA = 5+R1
      2. EA = R1
      3. EA = [R1]

d) EA = 5+[R1]

Ans:D

* 1. The extension that is essential for every assembly level program is
     1. .ASP
     2. .ALP
     3. .ASM
     4. .PGM Ans:C
  2. The logic operations are implemented using circuits.
     1. Bridge
     2. Logical
     3. Combinatorial
     4. Gate Ans: C
  3. The product of 1101 & 1011 is

a) 10001111

b) 10101010

c) 11110000

d) 11001100

Ans:A

* 1. The method used to reduce the maximum number of summands by half is
     1. Fast multiplication
     2. Bit-pair recording
     3. Quick multiplication
     4. Booth pair Ans: B
  2. The multiplier -6(11010) is recorded as a) 0-1-2

b) 0-1+1-10

c) -2-10

d) 0 1 1

Ans:A

9.A word whose individual represent a control signal is A)Command

B) Control C)Co-ordination D)Generation

Answer: B

1. The fetch and execution cycles are interleaved with the help of

A)Modification in processor Architecture B)clock

1. Special unit
2. Control Unit Answer: B
3. Individual control words of a micro routine are called as
4. Micro Task
5. Micro Operation
6. Micro Instruction
7. Micro Command Answer: C
8. The periods of time when the unit is idle is called as

A)Stalls

B)Bubbles C)Hazards

D)Both Stalls and Hazards. Answer: D

1. Goal of software techniques and hardware techniques, is to exploit
   1. Parallelism
   2. Scalability
   3. Supervision
   4. Compatibility ANSWER:A
2. On-chip memory which is local to every multithreaded Single Instruction Multiple Data (SIMD) Processor is called
   1. Flash Memory
   2. Global Memory
   3. Local memory
   4. Stack Answer: C
3. Memory management on a multiprocessor must deal with all of found on
4. Computer
5. Uniprocessor Computer C)Processor

D)System Answer: B

1. If node having a copy of a cache block, this technique is known as A)Uniform memory access

B)Cached

C)Un-cached D)Commit. Answer:C

1. Which of the following is not a write policy to avoid Cache Coherence?
2. Write through
3. Write within
4. Write back
5. Buffered write Ans:B
6. In mapping, the data can be mapped anywhere in the Cache Memory.
7. Associative
8. Direct
9. Set Associative
10. Indirect Ans:a
11. Separation of user logical memory and physical memory is
12. Memory control
13. Memory management
14. Memory sharing
15. Virtual memory ans:d
16. Levels between CPU and main memory were given a name of
    1. Hit time
    2. Miss rate
    3. Locality in time
    4. Cache

Ans:D

**15CS203 - COMPUTER SYSTEM ARCHITECTURE**

Third Semester/Second Year

**OBJECTIVE TYPE QUESTION**

*Prepared by: Partha Sarathi Chakraborty, Assistant Professor, CSE*

**Objective Type Questions UNIT – 1 1 mark each**

1. In case of zero address instruction method the operands are stored in
   1. Registers (b) Accumulator

(c) Stack (d) Cache

1. The register used to store the flags is called
   1. Flag register (b) Status register

(c) Tag register (d) Code register

1. The smallest entity of memory is known as
2. The instructions like MOVE or ADD are called as
   1. Opcode (b) Operator

(c) Command (d) Variable

1. The effective address of the operand is generated by adding a constant value to the contents of a register was
   1. Immediate mode (b) Index mode

(c) Indirect mode (d) Relative mode 4.The arrangement in which some memory address

values are used to refer to peripheral device buffer

registers known as

1. Memory Mapped I/O
2. Program Controlled I/O
3. Device Interface
4. Cache Arrangement
   1. collection of lines that connects several devices is called
      1. Data Bus (b) Internal Wires
5. Bus (d) Connection Wires
   1. Cell (b) Block (c) Word (d) Byte
6. Identify two phases of executing an instruction are
   1. Decode and Storage
   2. Fetch and Decode
   3. Fetch and Execute
   4. Decode and Execute
7. Refering to the operational units and their intercon- nections that realize the architectural specifications is known as
   1. Computer Architecture
   2. Computer Organization
   3. Computer Hardware
   4. Computer System
8. holds the address of the location to be accessed.
   1. MDR (b) MBR (c) MAR (d) PC

**Objective Type Questions UNIT – 1 mark each**

1. The method used to reduce the maximum number of summands by half is
   1. Bit-Recoding (b) Carry-Lookahead Logic

(c) Bit-Pair Recoding (d) Carry-Save Addition 12.In IEEE 64 bit representation, the exponent of a floating point number is said to occupy

bits.

(a) 8 (b) 9 (c) 10 (d) 11

1. In standard IEEE floating point number represen- tation, exponent is represent as a
   1. 2’s complement representation
   2. 1’s complement representation
   3. Biased representation
   4. Sign-Magnitude representation
2. The multiplier 122 (01111010) can be represent in bit recoding booth algorithm as

(a) M *×*(26 + 25 + 24 + 23 + 21)

(b) M *×*(27 *−* 23 *−* 21)

(c) M *×*(27 *−* 23 + 22 *−* 21)

(d) M *×*(*−*23 + 22 *−* 21)

1. Which approach can be taken to reduce delay in adders?
   1. Carry Save Adder
   2. n-bit Ripple-Carry Adder
   3. Cascade of k n-bit Adder
   4. Carry-Lookahead Adder
2. When period is placed to the right of first signifi- cant digit, the number is said to be
   1. Scale factor (b) Denormal

(c) Normalized (d) Unnormalized

1. The way of removing the guard bits and no changes in retained bits is called as
   1. Rounding (b) Von Neumann Rounding

(c) Chopping (d) Sticky bit

1. Identify the bit-recoding set (+1, 1) is equivalent to bit-pair recoding

(a) (0, +1) (b) (*−*1, 0)

(c) (0, *−*1) (d) (+1, 0)

1. What will be the delay at 16 bit carry-lookahead adder built by four 4-bit carry-lookahead adder, if each gate level stage delay = 0.001*µ*s.

(a) 17, 18 (b) 7, 8 (c) 9, 10 (d) 7, 10

1. In signed-magnitude binary division, if the dividend is (11100)2 and divisor is (10011)2 then the result is

(a) (00100)2 (b) (10100)2

(c) (11001)2 (d) (01100)2

Page 1 of 3

**Objective Type Questions UNIT – 1 mark each**

* 1. word whose individual bits represent a control signal is
     1. Command word (b) Signal word

(c) Control word (d) Counter word 22.The microroutines for all instructions are stored in

a special memory called

(a) *µ*-routine store (b) Control word

(c) Instruction word (d) Control store 23.What do you mean by *bubbles* in the pipeline?

(a) Hazard (b) Stalls

(c) Side effect (d) Penalty

1. The condition in which either source or destination operands are unavailable during pipeline is known as
   1. Data hazard (b) Structural hazard

(c) Control hazard (d) Instruction hazard 25.The register that holds the result of ALU is

(a) Y (b) Z (c) R0 (d) TEMP

1. Identify the correct control sequence for increment PC
   1. *PCout, MARin, Select*4*, Add, Zin → Zout, PCin*
   2. *PCout, MARin, Read, Add, Zin → Zout, PCin*
   3. *PCout, MARin, Yin, Add, Zin → Zout, PCin*
   4. *PCout, MARin, Select*4*, Add, Yin → Yout, PCin*
2. Pipeline increases the CPU performance through increase its
   1. Efficiency (b) Latency

(c) Throughput (d) Both (a) and (c) 28.Highly encoded schemes that use compact codes to

specify only a small number of control functions in

each microinstruction are referred as a

1. Horizontal Organization
2. Vertical Organization
3. Compact Organization
4. Field-encoded Organization
5. The branch prediction decision may change depend- ing on execution history is called
   1. Dynamic branch prediction
   2. Speculative branch prediction
   3. Static branch prediction
   4. Delayed branch prediction
   5. technique called can minimize the penalty incurred as a result of conditional branch instructions.
      1. Branch prediction
      2. Dynamic branch prediction
      3. Delayed branching
      4. Branch folding

**Objective Type Questions UNIT – 1 mark each**

1. Block of cache are grouped into sets and mapping allows block of main memory to reside in any block of specific set is
   1. Cache mapping
   2. Associative mapping
   3. Direct mapping
   4. Set associative mapping
2. Which of the following terms describe that the in- formation which will be used in near future is likely to be in use already?
   1. Spatial Locality (b) Temporal Locality

(c) Least Recently Used (d) Hit ratio 33.What is LRU algorithm?

1. Pages out that have been used recently
2. Pages out that have not been used recently
3. Pages out the first page in given data
4. Pages out that have been least used recently 34.Which of the following is true about ROM?
5. It is faster to access than RAM.
6. It is non-volatile memory.
7. It stores more information than RAM.
8. It is used for cache memory.
9. In write operation, protocol updated simultaneously cache location and the main mem- ory location.
   1. Early restart (b) Write-back

(c) Write-through (d) Copy-back

* 1. cache that can support multiple outstanding misses is called
     1. Write Buffer (b) Prefetching

(c) Lockup-Free Cache (d) Virtual Memory 37.What is page table base register?

1. It holds starting address of page frame
2. It holds address of a page
3. It holds starting address of page table
4. It holds address of virtual page number
   1. special hardware unit that translates virtual ad- dresses into physical addresses is
      1. Memory Controller
      2. Memory Management Unit
      3. Direct Memory Access
      4. Translation Lookaside Buffer
5. The amount of time that elapses after the head is positioned over the correct track until the starting position of the addressed sector passes under the read/write head called
   1. Rotational delay (b) Access time

(c) Intersector delay (d) Seek time

1. The amount of time required to transfer a word of data to or from the memory is called
   1. Seek Time (b) Memory Latency

(c) Delay Time (d) Response Time

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**Objective Type Questions UNIT – 1 mark each**

1. All the bits of a byte are transferred simultaneously within the time-frame allotted for the transmission is known as
   1. Sequential Data Transfer Mode
   2. Serial Data Transfer Mode
   3. Parallel Data Transfer Mode
   4. Synchronous Data Transfer Mode
   5. bus may be driven by more than one source at different time intervals, the driver/buffer should be a tristate device with
      1. 0, 1, or *z*

(b) 00, 01, or 10

1. 0, *z*, *z*¯
2. 0, 1, or *z*¯
   1. single chip LSI device is used to interface serial IO to a parallel bus structure called
      1. SMART (b) UART

(c) INTR (d) Intel 82C55A

1. flag if any one of the two stop bits is 0.
   1. Framing Error (b) Parity Error

(c) Overrun Error (d) Interrupt Error

* 1. low cost, processor-independent bus that housed on the motherboard of a computer and used to con- nect I/O interfaces for a wide variety of devices. A device connected to it, appears to the processor as if it is connected directly to the processor bus. The bus known as
     1. PCI (b) SAS (c) SCSI (d) SATA

1. When large volumes of data are to be moved, a more efficient technique is required called
   1. Programmed IO (b) Interrupt-driven IO

(c) IO controller (d) Direct Memory Access

1. refers to the exceptional event which causes the CPU to temporarily suspend the current program being executed.
   1. Polling (b) Error

(c) Interrupt (d) Acknowledge

1. An IO channel also referred as is a processor equipped with more facilities than those are available in a typical DMA controller.
   1. Interrupt controller
   2. IO Control Unit
   3. Peripheral Processor Unit
   4. IO Processing Unit
2. When the processor detects an interrupt, it branches to an interrupt-service routine whose job it is to poll each I/O module to determine which module caused the interrupt. The poll could be in the form of a separate command line. It is known as
   1. Hardware Poll (b) Software Poll

(c) IO Poll (d) Vector Interrupt Poll 50.It has been adopted as IEEE Standard 1394 and it

uses differential point-to-point serial links.

(a) USB (b) FireWire

(c) SATA (d) PCI Express

**ANSWER OF OBJECTIVE TYPE QUESTION**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 1.(c) | 11.(c) | 21.(d) | 31.(d) | 41.(c) |
| 2.(a) | 12.(d) | 22.(d) | 32.(b) | 42.(a) |
| 3.(b) | 13.(c) | 23.(b) | 33.(d) | 43.(b) |
| 4.(c) | 14.(c) | 24.(a) | 34.(b) | 44.(a) |
| 5.(c) | 15.(c) | 25.(b) | 35.(c) | 45.(a) |
| 6.(b) | 16.(c) | 26.(a) | 36.(c) | 46.(d) |
| 7.(a) | 17.(c) | 27.(d) | 37.(c) | 47.(c) |
| 8.(c) | 18.(a) | 28.(b) | 38.(b) | 48.(c) |
| 9.(b) | 19.(d) | 29.(a) | 39.(a) | 49.(b) |
| 10.(c) | 20.(b) | 30.(c) | 40.(b) | 50.(b) |

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1. The serial port is used to connect basically and processor. a)I/Odevices

b)Speakers c)Printer d)Monitor Answer:a

1. UART stands for

a)Universal Asynchronous Relay Transmission. b)Universal Accumulator Register Transfer.

1. Universa lAsynchronous Receiver Transmitter.
2. None of the above.

Answer:c

1. The data transfer in UART is done in . a)Asynchronous start stop format

b)Synchrnous start stop format c)Isochronous format d)EBDIC format

Answer:a

1. In micro-programmed approach, the signals are generated by . a)Machine instructions
2. System programs
3. Utility tools
4. None of the above

Answer:a

1. A sequence of control words corresponding to a control sequence is called . a)Micro routine
2. Micro function
3. Micro procedure d)Noneoftheabove

Answer:a

1. The DMA transfers are performed by a control circuit called as a)Device interface
2. DMA controller
3. Data controller d)Overlooker

Answer:b.

1. After the complition of the DMA transfer the processor is notified by a)Acknowledge signal

b)Interrupt signal c)WMFC signal

d)None of the above

Answer:b.

1. The controller is connected to the
   1. Processor BUS
   2. System BUS
   3. External BUS
   4. None of the above

Answer:b

1. The DMA transfer is initiated by
   1. Processor
   2. The process being executed
   3. I/O devices
   4. OS

Answer:c

1. The techniques which move the program blocks to or from the physical memory is called as

.

* 1. Paging
  2. Virtual memory organisation
  3. Overlays
  4. Framing Answer:b.

1. is used to implement virtual memory organisation.
   1. Page table
   2. Frame table
   3. MMU
   4. None of the above

Answer:c

1. translates logical address into physical address.
   1. MMU
   2. Translator
   3. Compiler
   4. Linker

Answer:a.

.13) The asscociatively mapped virtual memory makes use of .

1. TLB
2. Page table
3. Frame table
4. None of the above

Answer:a

1. Each stage in pipelining should be completed within cycle.
   1. 1
   2. 2
   3. 3
   4. 4

Answer:a

1. The periods of time when the unit is idle is called as .
   1. Stalls
   2. Bubbles
   3. Hazards
   4. Both a and b Answer:d
2. The situation where in the data of operands are not available is called .
   1. Data hazard
   2. Stock
   3. Deadlock
   4. Structural hazard

Answer:a.

1. The advantage of I/O mapped devices to memory mapped is
   1. The former offers faster transfer of data
   2. The devices connected using I/O mapping have a bigger buffer space
   3. The devices have to deal with fewer address lines
   4. No advantage as such

Answer:c.

1. The method of accessing the I/O devices by repeatedly checking the status flags is
   1. Program-controlled I/O
   2. Memory-mapped I/O
   3. I/O mapped
   4. None

View Answer

Answer:a.

1. The process where in the processor constantly checks the status flags is called as
   1. Polling
   2. Inspection
   3. Reviewing
   4. Echoing

View Answer Answer:a

1. What does the hardwired control generator consist of ?
   1. Decoder/encoder
   2. Condition codes
   3. Control step counter
   4. All of the above Answer:d
2. What are the major characteristics of a pipeline? (4m)

The major characteristics of a pipeline are:

1. Pipelining cannot be implemented on a single task, as it works by splitting multiple tasks into a number of subtasks and operating on them simultaneously.
2. The speedup or efficiency achieved by suing a pipeline depends on the number of pipe stages and the number of available tasks that can be subdivided.
3. If the task that can be subdivided has uneven length of execution times, then the speedup of the

pipeline is reduced.

1. Though the pipeline architecture does not reduce the time of execution of a single task, it reduces the overall time taken for the entire job to get completed.
2. What is the use of cache memory? (Explanation and cache memory and main memory diagram) 4m

The use of the cache memories solves the memory access problem. In particular, when a cache is included on the same chip as the processor, access time to cache is usually the same as the tine needed to perform other basic operations inside the processor. This makes it possible to divide instruction fetching and processing into steps that are more or less equal in duration. Each of these steps is performed by a different pipeline stages, and the clock period is chosen to correspond to the longest one.

1. a) What is locality of reference?(2m) b)What are called stalls?
2. Analysis of program shows that many instructions ion localized areas of the program are executed

repeatedly during some time period, and the remainder of the program, accessed relatively infrequently. This is referred to as locality of reference. This property leads to the effectiveness of cache mechanism.

1. An alternative representation of the operation of a pipeline in the case of a cache miss gives the function performed by each pipeline stage in each clock cycle. The periods in which the decode unit, execute unit and the write unit are idle are called stalls. They are also referred to as bubbles in the pipeline.
2. Describe the memory hierarchy?compare in terms of size ,speed and cost with diagram(4m) Processor (2m and diagram 2m)

Registers

Primary Cache Secondary Cache Main memory

Magnetic disk secondary

1. a)What are the objectives of USB?(2m)

* Simple
* Low cost
* Easy to use
* Supports wide range of data transfer characteristics.
* Plug and play mode of operation

1. what are the various mechanisms for implemernting I/O operations? (2m)

* Program controlled I/O
* Interrupts
* DMA

Unit 5 MCQ

Transfer of data directly between a peripheral and memory without the aid of cpu is achieved using

* 1. NMI controller
  2. DDR controller
  3. **DMA controller**
  4. None of the above

Block Transfer from memory will be beneficial due to which of the following?

1. Spatial Locality
2. Lesser Memory Latency
3. Paging
4. **All of the above**

The presence of a page in a cache is detected by checking the

1. Valid bit
2. Dirty bit
3. **Tag bit**
4. None of the above

The Translation Look Aside Buffer (TLB) stores

1. Branching data
2. Map of Cache data and RAM data
3. **Map of Physical Address and Logical Address**
4. Memory Translation times

In general, a single DRAM memory cell contains

1. single capacitor and multiple transistors.
2. multiple capacitors and single transistor.
3. **single capacitor and single transistor.**
4. multiple capacitors and multiple transistors.

Assume the data bus width of DDR memory system is 32 bits. How many cycles does it take to transfer 64B cache block?

1. 64
2. 16
3. **8**
4. 1

A CPU generally handles an interrupt by executing an interrupt service routine

1. As soon as an interrupt is raised
2. By checking the interrupt register at the end of fetch cycle
3. **By checking the interrupt register after finishing the execution of the current instruction**
4. By checking the interrupt register at fixed intervals.

A hard disk with 5 platters has 2048 tracks/platter, 1024 sectors/track (fixed number of sectors per track), and 512 byte sectors. What is its total capacity?

1. 7GB
2. **5GB**
3. 4GB
4. 8GB

Which among the following is true?

1. **The memory allocated to each page is contiguous.**
2. The offset is different in a virtual address and a physical address
3. Logical address space can be smaller than physical address space
4. Segmentation avoids external memory fragmentation

Page fault occurs when

1. a requested page is in memory
2. **a requested page is not in memory**
3. a page is corrupted
4. None of the above

In which mapping, the data can be mapped anywhere in the cache memory?

1. **Associative**
2. Direct
3. Set Associative
4. Indirect

Which cache write mechanism allows an updated memory location in the cache to remain out of date in memory until the block containing the updated memory location is replaced in the cache?

1. Write through
2. **Write back**
3. Both write through and write back
4. Cycle Stealing

The address of a page table in memory is pointed by

1. stack pointer
2. page table base register
3. page register
4. **program counter**

Memory management technique in which system stores and retrieves data from secondary storage for use in main memory is called

1. Fragmentation
2. **Paging**
3. Mapping
4. Indexing

Cache memory

1. has greater capacity than RAM
2. is faster to access than CPU Registers
3. is permanent storage
4. **faster to access than RAM**

**When does the input devices send information to the processor?**

1. When the data arrives regardless of the SIN flag
2. **When the SIN status flag is set**
3. When the Sout status flag is set
4. When the data arrives regardless of the Sout flag

**An interface that provides a method for transferring binary information between internal storage and external devices is called**

1. **I/O Interface**
2. DMA
3. DDR
4. Input Interface

**On receiving an interrupt from an I/O device, the CPU**

1. halts for predetermined time
2. **branches off to the interrupt service routine after completion of the current instruction**
3. branches off to the interrupt service routine immediately
4. hands over control of address bus and data bus to the interrupting device

**An interrupt can be temporarily ignored by the counter is called**

1. Vector interrupt
2. Non maskable interrupt
3. **Maskable interrupt**
4. Low priority interrupt

**Of the following, which best characterizes computers that use memory-mapped I/O?**

1. The computer provides special instructions for manipulating I/O ports.
2. **I/O ports are placed at addresses on the bus and are accessed just like other memory locations.**
3. To perform an I/O operation, it is sufficient to place the data in an address register and call the channel to perform the operation.
4. Ports are referenced only by memory-mapped instructions of the computer and are located at hardwired memory locations.

A process is thrashing if :

1. it spends a lot of time executing, rather than paging
2. it has no memory allocated to it
3. **it spends a lot of time paging, than executing**
4. None of these

Run time mapping from virtual to physical address is done by

1. **Memory management unit**
2. CPU
3. PCI
4. none of the mentioned

I/O hardware contains

1. bus
2. Controller
3. I/O port and its registers
4. **all of the mentioned**

In transfer each bit is sent one after theanother in a sequence of event and requires just one line:

1. **Serial**
2. Parallel
3. Both a & b
4. None of these

In technique has 1 or more controlsignal for acknowledgement that is used for intimation:

1. **Handshaking**
2. Strobe
3. Both a & b
4. None of these

is a single address space for storingboth memory and I/O devices:

1. **Memory-mapped I/O**
2. Isolated I/O
3. Separate I/O
4. Optimum I/O

is a single control line that informsdestination unit that a valid is available on the bus:

* 1. **Strobe**
  2. Handshaking
  3. Synchronous
  4. Asynchronous

Which technique is used that identifies thehighest priority resource by means of software:

1. Daisy chaining
2. **Polling**
3. Priority
4. Chaining

Which exception is also called softwareinterrupt:

1. Interrupt
2. **System calls**
3. Traps
4. All of these

Each interaction b/w CPU and I/O moduleinvolves:

1. **Bus arbitration**
2. Bus revolution
3. Data bus
4. Control signals

Which are 4 types of commands received byan interface:

1. **Control, status, data output, data input**
2. Only data input
3. Control, flag, data output, address arbitration
4. Data input, data output, status bit, decoder